**Experiment-8 DT-17.11.2020**

**Aim** :

To design SISO,SIPO,PIPO and PISO shift registers and test them.

**Apparatus required :**

1) Tinkercad Software

2) Breadboard

3) Power Supply

4) Slideswitch

5) AND gate 74HC08

6) HEX INVERTER gate 74HC04

7) OR gate 74HC32

6) DUAL JK FF gate 74HC73

7) Resistors

8) LEDs

9) Connecting wires

**Theory :**

To increase the storage capacity in terms of number of bits, we have to use a group of flip-flop. Such a group of flip-flop is known as a **Register**. The **n-bit register** will consist of **n** number of flip-flop and it is capable of storing an **n-bit** word.

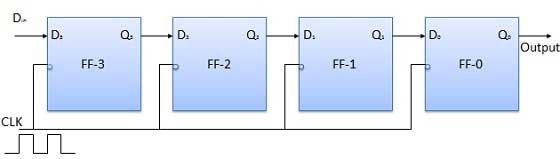
The binary data in a register can be moved within the register from one flip-flop to another. The registers that allow such data transfers are called as **shift registers**. There are four mode of operations of a shift register.

* Serial Input Serial Output
* Serial Input Parallel Output
* Parallel Input Serial Output
* Parallel Input Parallel Output

Serial Input Serial Output

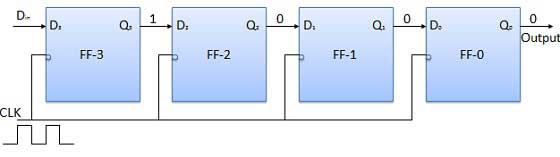
Let all the flip-flop be initially in the reset condition i.e. Q3= Q2= Q1 = Q0= 0. If an entry of a four bit binary number 1 1 1 1 is made into the register, this number should be applied to**Din**bit with the LSB bit applied first. The D input of FF-3 i.e. D3is connected to serial data input **Din**. Output of FF-3 i.e. Q3 is connected to the input of the next flip-flop i.e. D2 and so on.

Block Diagram

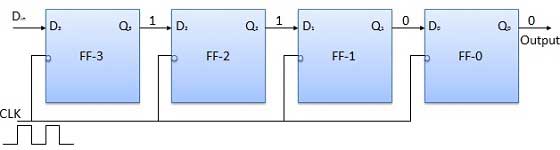


Operation

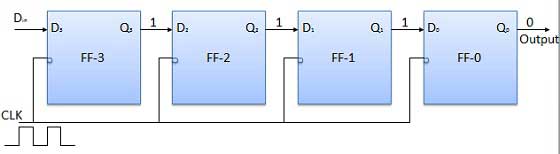
Before application of clock signal, let Q3 Q2 Q1 Q0 = 0000 and apply LSB bit of the number to be entered to Din. So Din = D3 = 1. Apply the clock. On the first falling edge of clock, the FF-3 is set, and stored word in the register is Q3 Q2 Q1 Q0 = 1000.



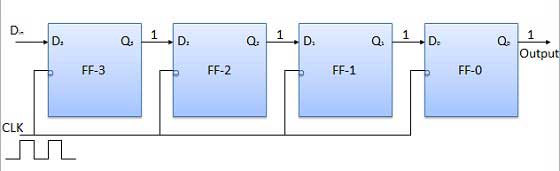
Apply the next bit to Din. So Din = 1. As soon as the next negative edge of the clock hits, FF-2 will set and the stored word change to Q3 Q2 Q1 Q0 = 1100.



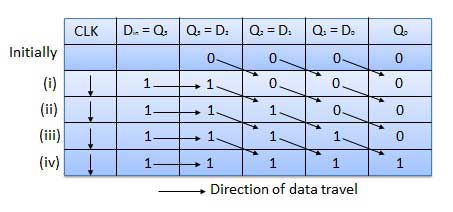
Apply the next bit to be stored i.e. 1 to Din. Apply the clock pulse. As soon as the third negative clock edge hits, FF-1 will be set and output will be modified to Q3Q2Q1 Q0 = 1110.



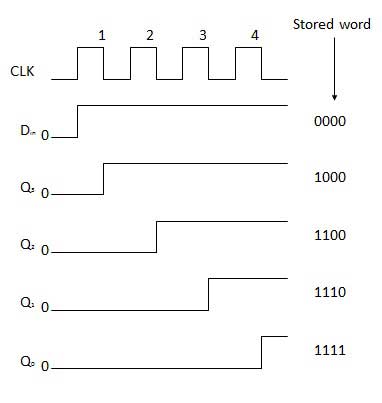
Similarly with Din= 1 and with the fourth negative clock edge arriving, the stored word in the register is Q3Q2Q1Q0= 1111.



Truth Table



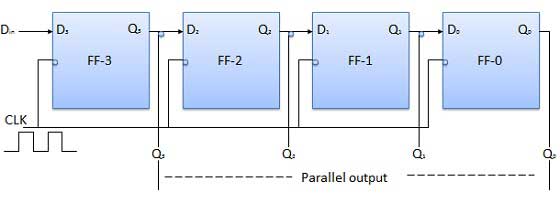
Waveforms



Serial Input Parallel Output

* In such types of operations, the data is entered serially and taken out in parallel fashion.
* Data is loaded bit by bit. The outputs are disabled as long as the data is loading.
* As soon as the data loading gets completed, all the flip-flops contain their required data, the outputs are enabled so that all the loaded data is made available over all the output lines at the same time.
* 4 clock cycles are required to load a four bit word. Hence the speed of operation of SIPO mode is same as that of SISO mode.

Block Diagram



Parallel Input Serial Output (PISO)

* Data bits are entered in parallel fashion.
* The circuit shown below is a four bit parallel input serial output register.
* Output of previous Flip Flop is connected to the input of the next one via a combinational circuit.
* The binary input word B0, B1, B2, B3 is applied though the same combinational circuit.
* There are two modes in which this circuit can work namely - shift mode or load mode.

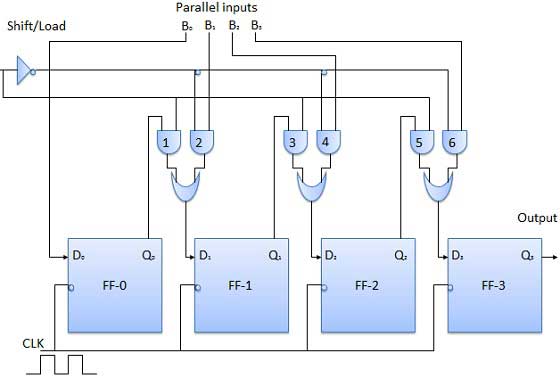
Load mode

When the shift/load bar line is low (0), the AND gate 2, 4 and 6 become active they will pass B1, B2, B3 bits to the corresponding flip-flops. On the low going edge of clock, the binary input B0, B1, B2, B3 will get loaded into the corresponding flip-flops. Thus parallel loading takes place.

Shift mode

When the shift/load bar line is low (1), the AND gate 2, 4 and 6 become inactive. Hence the parallel loading of the data becomes impossible. But the AND gate 1,3 and 5 become active. Therefore the shifting of data from left to right bit by bit on application of clock pulses. Thus the parallel in serial out operation takes place.

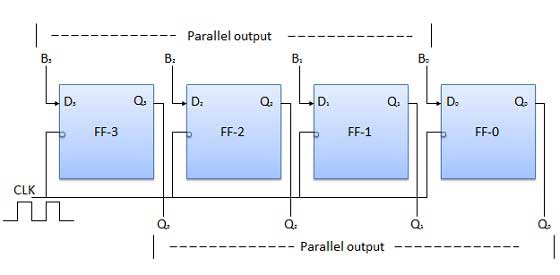
Block Diagram



Parallel Input Parallel Output (PIPO)

In this mode, the 4 bit binary input B0, B1, B2, B3 is applied to the data inputs D0, D1, D2, D3 respectively of the four flip-flops. As soon as a negative clock edge is applied, the input binary bits will be loaded into the flip-flops simultaneously. The loaded bits will appear simultaneously to the output side. Only clock pulse is essential to load all the bits.

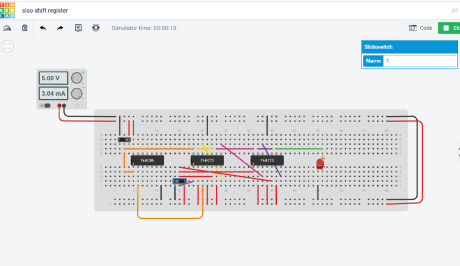
Block Diagram



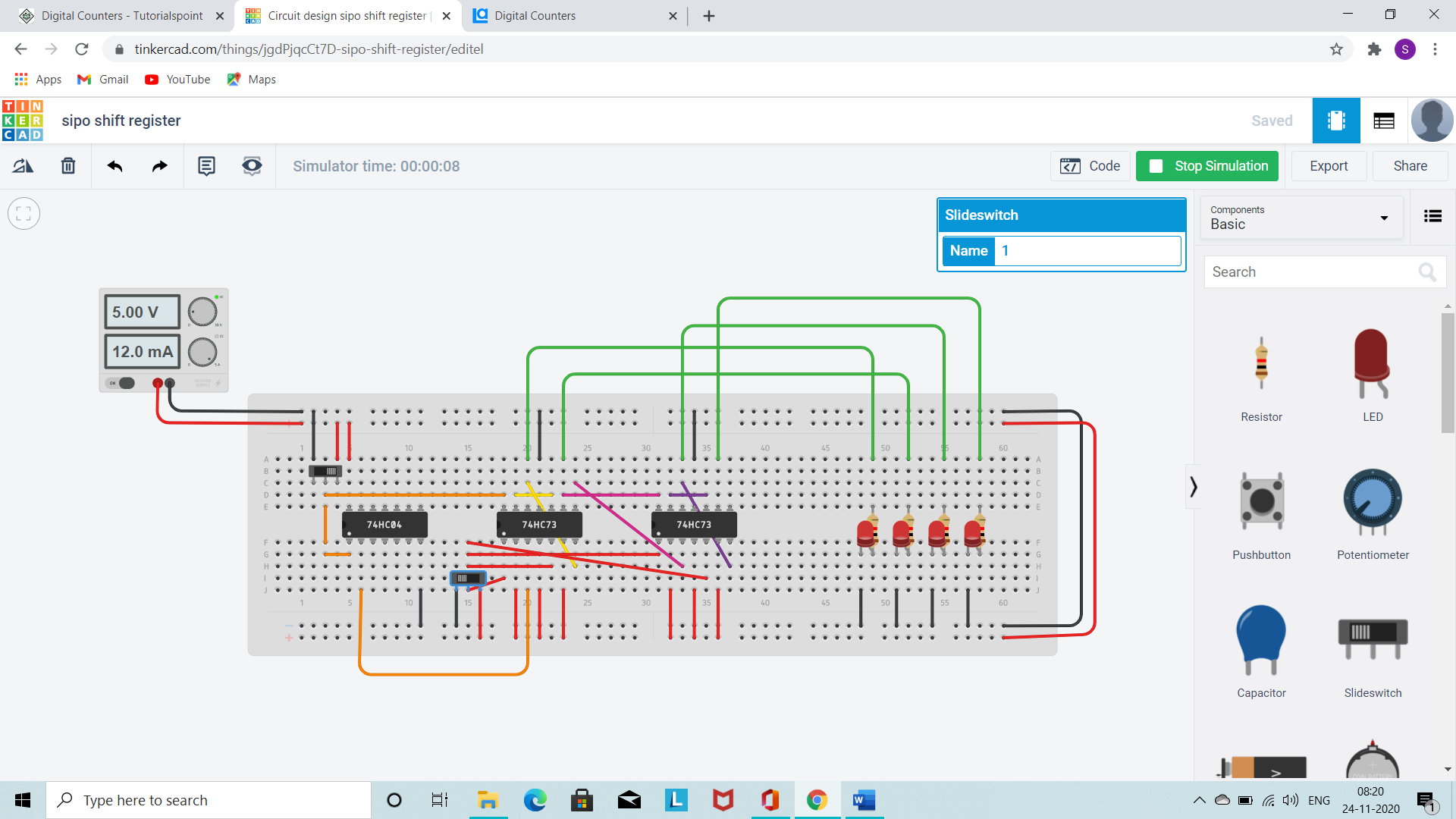
For JK flip flops, and D flip flops, we know that J= D and K=D’ respectively.

**Observation :**

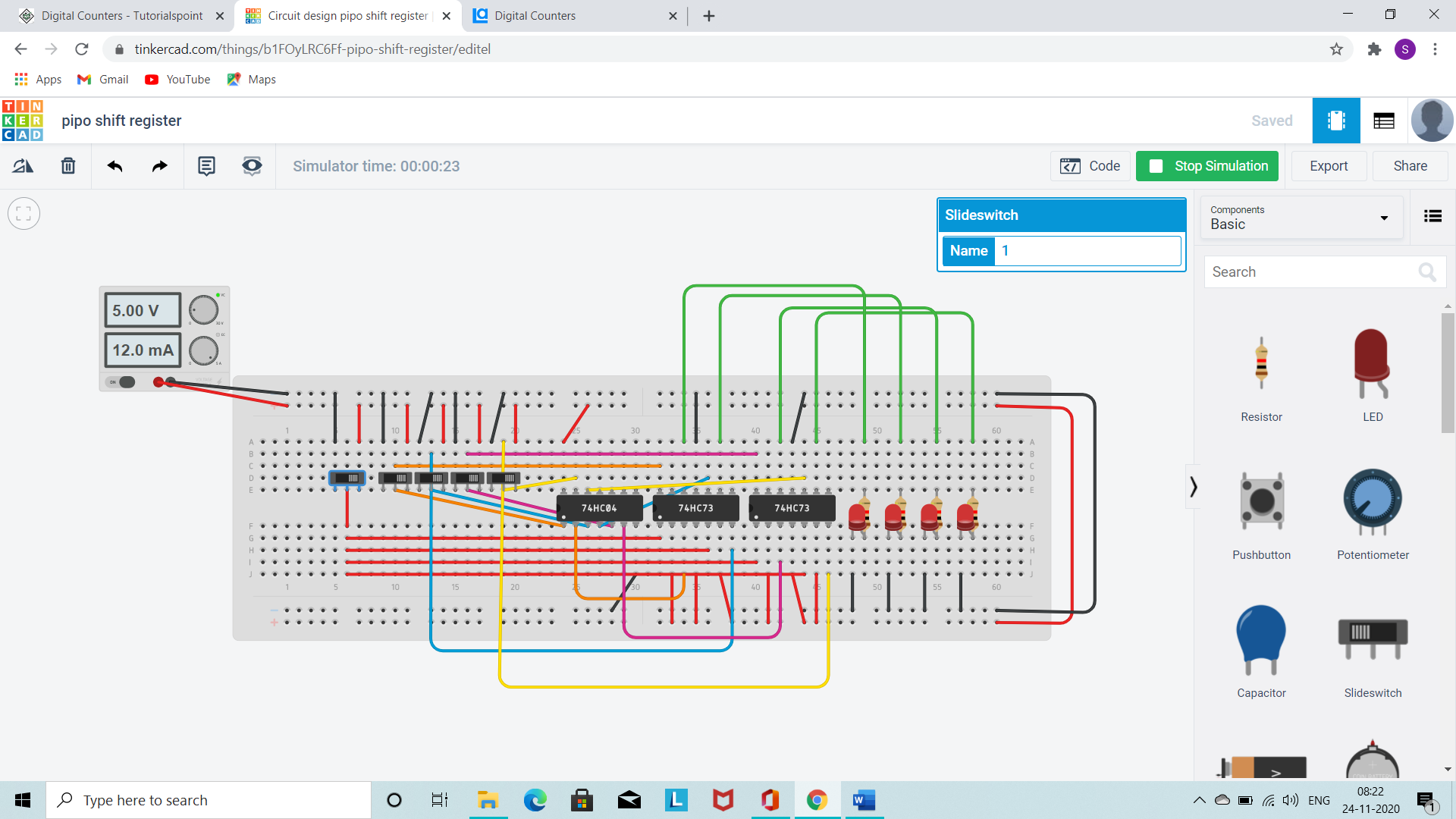
SISO



SIPO

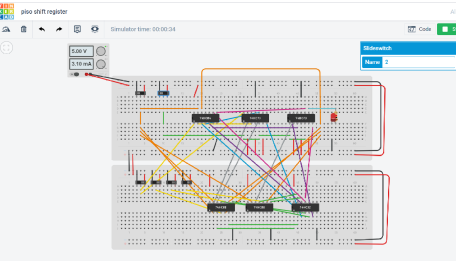


PIPO



PISO

When shift/load is 0/1, we can toggle clk and data input alternatively to get output or give all data inputs consecutively and then toggle clk to get output.



**Conclusion :**

All the circuits were designed and verified for all inputs.

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